

VLSI IMPLEMENTATION OF BACK PROPAGATED NEURAL NETWORK FOR SIGNAL PROCESSING

UJWALA A. KSHIRSAGAR (BELORKAR) & ASHISH E. BHANDE

H.V.P.M.'s College of Engineering & Technology, Amravati, Maharashtra, India

ABSTRACT

Mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI Technology, the number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power of these applications is the driving force for the fast development of this field. This paper presents the implementation of Neural Network for signal processing application using VLSI technology. Gilbert mixer which is a transistorized circuit used as an analog multiplier and Adder of Neural Network. The advantage of this circuit is the output current is an accurate multiplication of the (differential) base currents of both inputs. As a mixer, its balanced operation, cancels out many unwanted mixing products, resulting in a "cleaner" output. Through the proposed Neural Network, Compression & Decompression of two analog signals successfully implemented. Effort has been taken to design Neural Network for signal processing, using VLSI technology. VLSI Technology includes process design, trends, chip fabrication, real circuit parameters, circuit design, electrical characteristics, configuration building blocks, switching circuitry, translation onto silicon, CAD and practical experience in layout design. The proposed mixer is designed using 45 nm CMOS/VLSI technology with microwind 3.1.

KEYWORDS: Gilbert Mixer, Micro Wind 3.1, 45nm CMOS Technology, Compression, Decompression, Neural Network

INTRODUCTION

Artificial intelligence is realized based on mathematical equations and artificial neurons. In the proposed design, our main focus is on the implementation of chip layout design for Feed forward Neural Network Architecture (NNA) in VLSI for generic analog signal processing applications. The analog components like Gilbert Cell Multiplier (GCM), Adders, Neuron activation Function (NAF) are used in the implementation. This neural architecture is trained using Back propagation (BP) algorithm in analog domain with new techniques of weight storage. We are using 45nm CMOS technology for layout designing and verification of proposed neural network. The functionality of proposed design of neural network is verified for the analog operations like signal amplification and multiplication. Intelligence is the computational part of the ability to achieve goals in the world. This intelligence though a biological world is realized based on the mathematical equations, giving rise to the science of Artificial Intelligence (AI). To implement this intelligence artificial neurons are used.

These artificial neurons comprised of several analog components. The neuron selected is comprised of multiplier and adder along with the tan-sigmoid function. The training algorithm used is performed in analog domain thus the whole neural architecture is analog structure. The proposed technology is a step in the implementation of neural network

architecture using back propagation algorithm. These artificial neurons, are realized by Analog components like multipliers, adders and differentiators in 45nm CMOS VLSI technology.

Due to the rapid advances in integration technologies, large-scale systems design - in short and due to the advent of VLSI Technology the electronics industry has achieved a phenomenal growth over the last two decades. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising rapidly and consistently. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field.

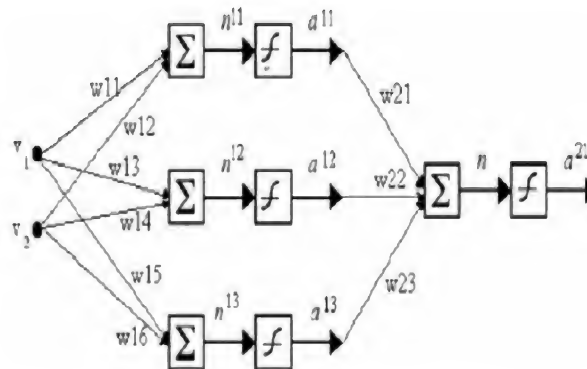


Figure 1: Layered Neural Network

The neural network is shown in figure 1. In this network, inputs v_1 , v_2 are applied with the weight matrix, then this weighted inputs of the adder are summed up. The output generated by adder blocks is given to the Neuron Activation function. The output of activation function is multiplied by weights again and given to the input blocks of output layer.

This layered structure of neural network is implemented in VLSI using analog components. Gilbert cell multiplier, adder and differential amplifier are used for different blocks. To reduce the power requirement we have designed the neural network using advanced technology. The human brain consists of neurons that send activation signals to each other thereby creating intelligent thoughts. The algorithmic version of a neural network (called an artificial neural network) also consists of neurons which send activation signals to one another. The end result is that the artificial neural network can approximate a function of multiple inputs and outputs. As a consequence, neural networks can be used for a variety of data mining tasks, among which are classification, descriptive modeling, clustering, function approximation, and time series prediction. Neural networks are also commonly used for image processing.

The proposed neural architecture will be capable of performing operations like sine wave learning, amplification and frequency multiplication and can also be used for analog signal processing activities.

Now a days, power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. Since the Gilbert's Mixer useful in frequency translation in communication system, it is needed to design MIXER for modern communication engineering applications with low power, high stability and low jitter. This paper introduces design aspects for layout design of **Gilbert cell** using VLSI technology.

The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirement. When the requirements are not met, the design has to be improved. More simplified view of the VLSI technology consists of various representations, abstractions of design, logic circuits, CMOS circuits and physical layout.

Here for the design, micro wind 3.1 VLSI Backend software is used. This software allows designing and simulating an integrated circuit at physical description level. The proposed Mixer is designed using 45 nm CMOS/VLSI technology in micro wind 3.1 software, which in turn offers high speed performance at low power.

The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric [4]. The effective gate length required for 45 nm technology is 25nm. Some of the key features of 45 nm technologies from various providers like TSMC, Fujitsu, and Intel are as given in table-I below.

Compared to 65-nm technology, 45 nm technologies must offer:

1. 30% increases in switching performance
2. 30 % reduction in Power consumption
3. 2 times higher density
4. 2 times reduction of the leakage between source and drain and through the gate oxide [4].

Table 1: Key Features of 45 nm Technology

Parameter	Value
VDD (V)	0.85-1.2 V.
Ioff N (nA/um)	5-100
Ioff P (nA/um)	5-100
Gate dielectric	SiON, HfO ₂
No. of metal layers	6-10

Considering the advantage of 45 nm technologies over 90 nm & 65 nm technologies, the proposed work is done with 45 nm technologies. Power consumption is a limiting factor in VLSI integration for portable applications. The resulting heat dissipation also limits the feasible packaging and performance of the VLSI chip. Since the dynamic power dissipation in synchronous digital integrated circuit is determined by CV^2f , reducing the supply voltage is an effective way to reduce power consumption of the modern electronic systems [5]. As the supply voltage scales down with the technology, any power supply noise on power and ground level affects the analog circuit performance more than before [6].

IMPLEMENTATION OF GILBERT CELL & NEURON ACTVATION FUNCTION OF PROPOSED NEURAL NET-WORK USING VLSI

The Gilbert Mixer (cell) is used as the multiplier block. The main building blocks of Gilbert cell are differential pair transistors and current mirror circuit. In the proposed work Gilbert cell acts as multiplier and adder blocks of Neural Network.

A mixer with a single-ended RF signal is called a single-balanced mixer. An example is shown on figure 1. This configuration is rarely used because it is more susceptible to noise in the LO signal. Its main drawback is the LO-IF feed through. That is, the LO signal could leak into the IF if the IF is not much lower than the LO frequency. The low pass filter following the mixer may not properly suppress the LO signal without affecting the IF signal.

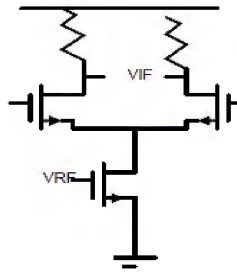


Figure 2: A Single-Balanced Mixer

Double Balanced Mixers are used to prevent the LO products from reaching the output. It is essentially two single-balanced circuits with the RF transistors connected in parallel and the switching pair in anti-parallel. Therefore, the LO terms sum to zero and the RF signal doubled in the output. This configuration provides a high degree of LO-IF isolation easing filtering requirements at the output. Double balanced mixers are less susceptible to noise than the single-balanced mixers because of the differential RF signal. Figure 3 shows a double balanced mixer, it is also known as the Gilbert Cell Mixer.

Mixers are used for frequency translation, they convert the RF frequency to the IF frequency by multiplying it with the LO frequency. This is shown in the result in figure 3. The mixing result produces two signal located at the LO+RF and LO-RF frequency. One signal is the wanted IF signal and the other is the unwanted signal as shown in equation.

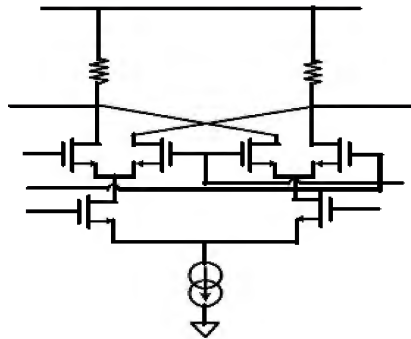


Figure 3: A Double Balanced Mixer

$$RF = A \cos (RF) * t \quad (1)$$

$$LO = B \cos (LO) * t \quad (2)$$

$$IF = A \cos (RF) * t + B \cos (LO) * t \quad (3)$$

$$IF = 1/2 * AB [\cos (LO + RF) * t + \cos (LO - RF) * t] \quad (4)$$

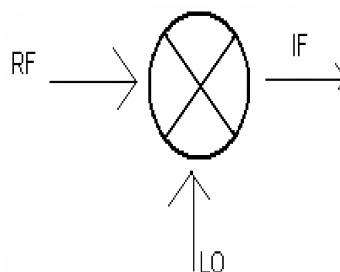


Figure 4: Mixers in Integrated Circuits

Proposed Neural Network uses transisterised Gilbert cell as shown in figure 5

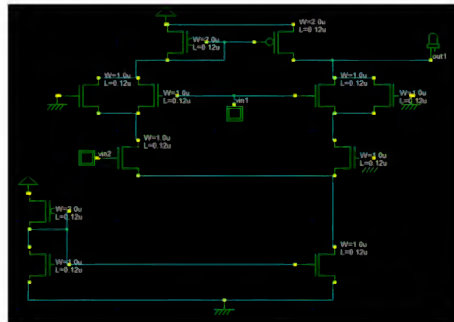


Figure 5: Schematic of Gilbert Cell

The figure 6 shows the layout of Gilbert cell which is designed using, 45nm VLSI technology & it is the first block of proposed design. The first input voltage signal V_{in1} is of 0.301V & the second input voltage signal V_{in2} is of 0.302V.

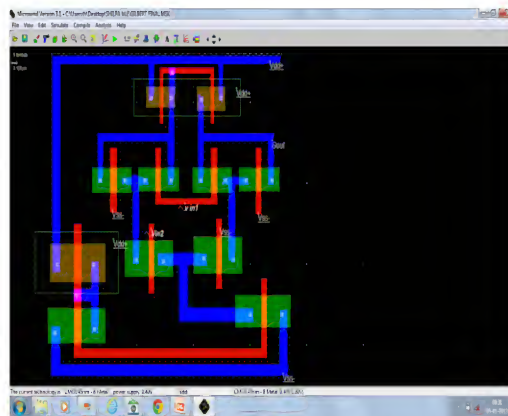


Figure 6: Chip Layout of Gilbert Cell

Figure 7 shows the voltage versus time response of Gilbert cell. Here output voltage obtained is 0.601V and power consumed by Gilbert cell is 11.964 μ W.

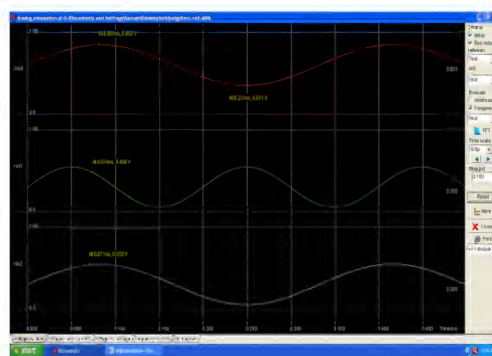


Figure 7: Voltage Versus Time Response of Gilbert Cell

In the proposed neural network we are using neuron activation function for validation. It will compare the input signal with the reference signal and then output will be generated. Neurons use sigmoid type activation functions. Complex surfaces can be described by simple networks using sigmoid type activation function. Nonlinear activation functions of neurons are essential for neural network operation. Such sigmoidal functions can be created in the differential pair. Figure 8 shows the schematic of neuron activation function. The layout of neuron activation function which is designed

using micro wind 3.1 software, 45nm CMOS technology is shown in Figure 9. The input voltage is 0.4V, low time is 0.090ns, high time is 0.090ns, rise time is 0.010ns & fall time is 0.010ns.

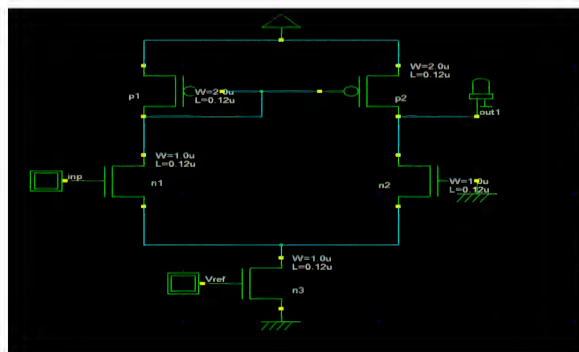


Figure 8: Schematic of Neuron Activation Function

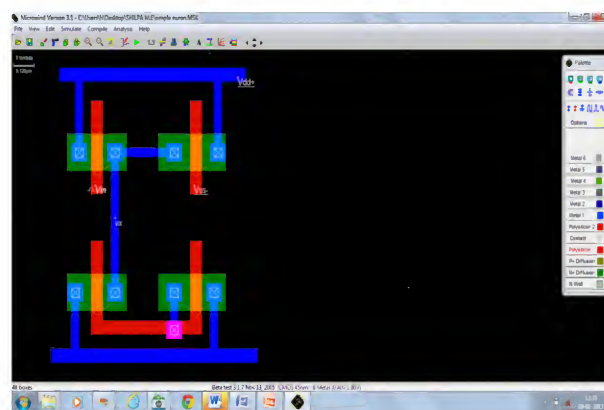


Figure 9: Layout of Neuron Activation Function

Following figure 10 shows the voltage versus time response of neuron activation function. Power consumed by neuron activation function is $3.533\mu\text{W}$.

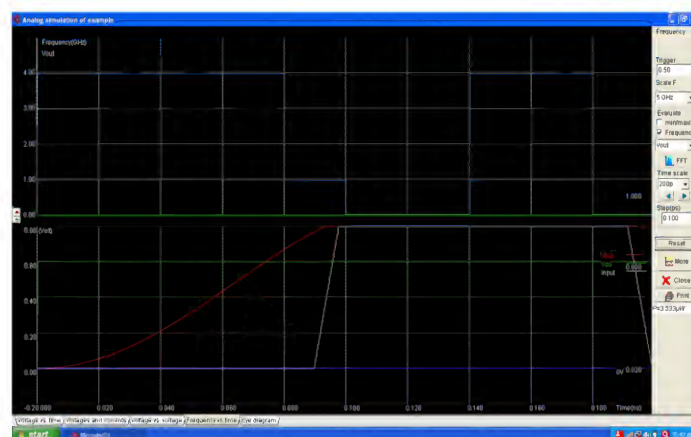


Figure 10: The Voltage versus Time Response

Neural Network Design for Signal Compression

Figure 11 shows the schematic of neural network design for signal compression. Here two analog signals are given as inputs and single signal is obtained at the output which is compressed signal.

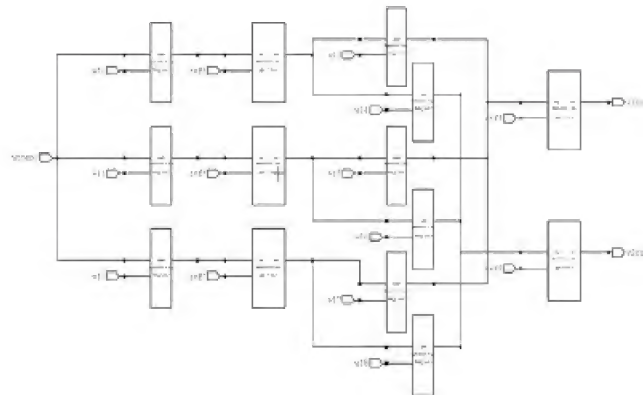


Figure 11: Schematic of Neural Network Design for Signal Compression

Figure 12 shows the layout of neural network design for signal compression. First input signal is of $V_{in1} = 0.500V$, second input is $V_{in2} = 0.500V$.

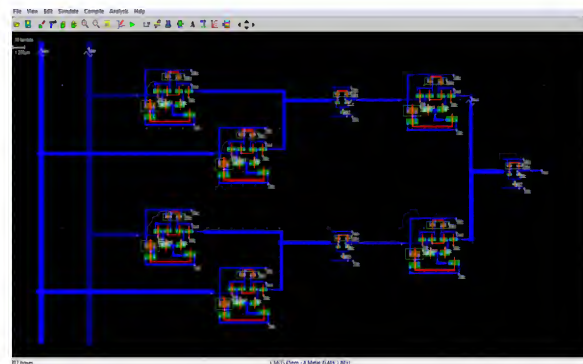


Figure 12: Layout of Neural Network Design for Signal Compression

Figure 13 shows the voltage versus time response of neural network design for signal compression. Here compressed signal obtained by neural network is $V_{out} = 0.300V$. Power required by the neural network for signal compression is $0.250mW$.

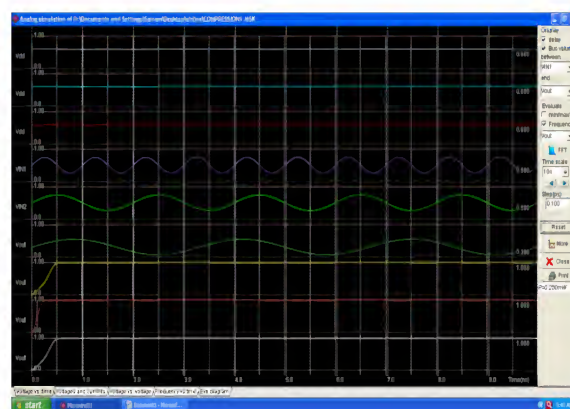


Figure 13: Voltage versus Time Response of Neural Network Design for Signal Compression

Neural Network Design for Signal Decompression

Figure 14 shows the schematic of neural network design for signal decompression. Here single analog signal is given as input, which is output generated by neural network for signal compression. Two output signals are produced which are same as inputs given to the neural network design for signal decompression.

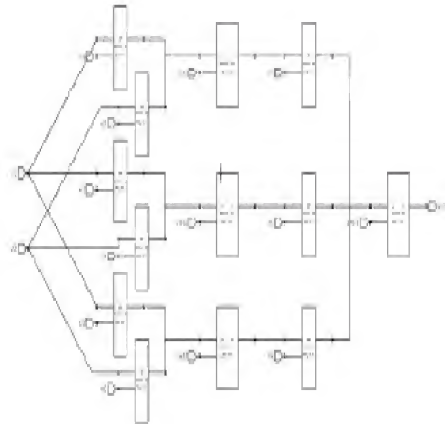


Figure 14: Schematic of Neural Network Design for Signal Decompression

The following figure 15 shows the layout of neural network for signal decompression which is designed using micro wind 3.1 software in 45nm CMOS technology. The input voltage signal is sinusoidal waveform of 0.518V.

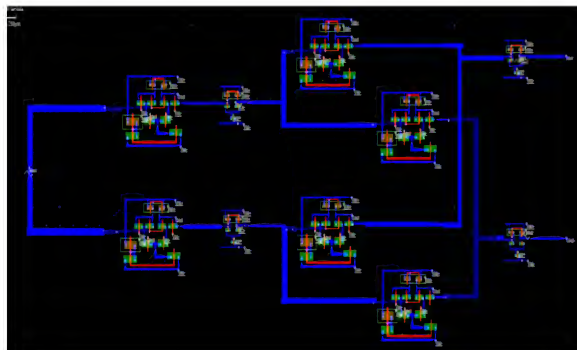


Figure 15: Layout of Neural Network for Signal Decompression

Both the output signal obtained after decompression is same as the two inputs of neural network for compression. The Power consumed by neural network is 0.274mW as shown in figure 16.

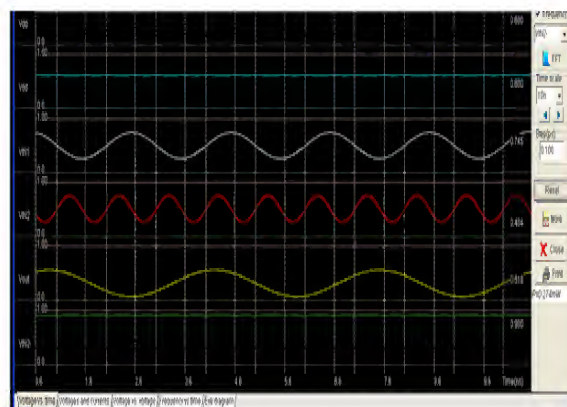


Figure 16: Output Response of Neural Network for Signal Decompression

CONCLUSIONS

Considering the advancement of future technology and the advantage of 45 nm technology over 65 and 90 nm technology, the selection of 45nm technology for the proposed neural network was the proper choice of technology. The VLSI implementation of a Back propagated neural network successfully implemented using 3.1 micro wind

(VLSI back-end) software. The two analog signal applied for compression successfully achieved at the output of decompression using back propagation algorithm technology.

REFERENCES

1. P. J. Sullivan, B. A. Xavier and W. H. Ku, "A low voltage performance of microwave CMOS Gilbert Cell Mixer," in *IEEE J. Solid-State Circuits*, vol. 32, pp1151-1155, July 1997.
2. B. Gilbert, "A high-performance monolithic multiplier using active feedback," *IEEE J. Solid-State Circuits*, vol. SC-9, pp.364-373 Dec.1974.
3. B. Song, "CMOS RF circuits for data communications application," *IEEE J. Solid- State Circuits*, vol. SC-21, pp. 310-317, Apr.1986.
4. E. Sicard, Syed Mahfuzul Aziz, "introducing 45 nm technology in Microwind3," micro wind application note
5. Navid Azizi, Student Member, IEEE, Muhammad M. Khellah, Member, IEEE, Vivek K. De, Senior Member, IEEE, and Farid N. Najm, Fellow, IEEE, "Aware Low-Power Design and Block." *IEEE transactions on very large scale integration (vlsi) systems*, vol. 15, no. 7, july 2007.
6. E. Sicard, S. Delman- Bendhia, "Deep submicron CMOS Design".
7. Jun Zhao, Yong –Bin Kim "A Low-Power Digitally Controlled Oscillator for All Digital Phase-Locked Loops" *VLSI Design Volume 2010*
8. B. M. Wilamowski, J. Binfet, and M. O. Kaynak "VLSI Implementation of Neural Networks"
9. Gilbert Multiplier by Ari Sharon, aris@cs, Ariel Zentner, relz@cs, Zachi Sharvit, zachi@cs, Yaakov Goldberg, yaakov@cs
10. Rafid Ahmed Khalil & Sa'ad Ahmed Al-Kazzaz "Digital Hardware Implementation of Artificial Neurons Models UsingFPGA"pp.12-24
11. Neeraj Chasta, Sarita Chouhan and Yogesh Kumar "Analog VLSI Implementation of Neural Network Architecture for Signal Processing"

